AMD

ULTRA LOW POWER HIGH SPEED CLOCK DISTRIBUTION

- A CASE FOR ITS USAGE IN ENERGY EFFICIENT MULTI-LANE PHY

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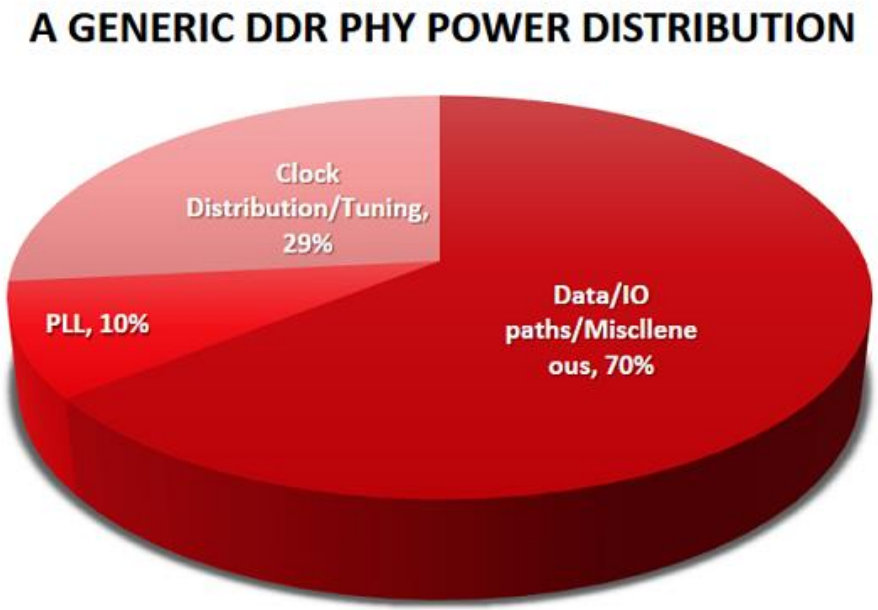
MOTIVATION

ENERGY EFFICIENCY, A KEY REQUIREMENT FOR PHY DESIGN

- Growth of data traffic is pushing the bandwidth requirements of communication servers but thermal limits/battery energy are making it power limited.
- Improved bandwidth and reduced latency are key performance parameters between processor & memory; recent focus has been on improvement in the communication speed and PHY plays a key role in this aspect with the following challenges:
  - *Minimal latency.*
  - *Maximum bandwidth.*
  - *Improved Energy Efficiency.*

CLOCK POWER VS JITTER IN PHY

- Clock switching remains one of the main source of power consumption in most commercial designs and the larger die size makes it worse.
  - Analysis showed Clock-Network power makes up a significant percentage of the total power in a generic DDR PHY (~29%).
- Jitter is also a critical aspect of the PHY design and impacted by the amplitude of clock at each stage.
  - Keeping the power consumption under check with decent signal amplitude (for low jitter) at high frequency is a challenge.
- Therefore, it is important to fine tune the design and strike a balance between power and jitter.
  - **This presentation discusses one efficient approach towards that.**



MAIN IDEA & CHALLENGE

CHALLENGES IN GLOBAL DISTRIBUTION OF CLOCK

- Let's look at a SERDES PHY design with a requirement of distributing high speed clock (6-8GHz) from central LC PLL to all Receiver (Rx)/ Transmitter(Tx) lanes over a span of 3mm. Key objectives included:
  - Adapting with changing dynamics of floorplan and downstream loading was a key challenge.
  - Closing design architecture, exploring multiple distribution schemes to get the best power efficiency.
  - EM/IR analysis closure; as clocks are always with high activity and require dense power grid distribution.
  - Route layer selection (without hurting SoC power grid) and Transmission-Line analysis.

KEY DESIGN CONSTRAINTS

- Design needed to strike a balance between power consumption, minimum input clock signal swing and Jitter specifications.
- Rx included phase based interpolator which has specific edge-rate/swing range requirements. PHY clock needed to support a wide range of frequency (1-8GHz).
  - Therefore, the designer also needed to provide swing and drive strength controllability option for different PVT (Process Voltage Temperature) and operative frequency.

All these goals, if met, should result in improved energy efficiency of the PHY

INITIAL CLOCK BUFFER ARCHITECTURE OPTIONS

- **CMOS Distribution**
  - For differential clock distribution at high frequency (~8Ghz), initial analysis showed rail to rail swing of CMOS distribution ends up burning lot of power; moreover, susceptibility to supply noise didn't make a promising case.
- **Current Mode Logic (CML) Distribution**
  - CML distribution is generally treated as the de-facto low power topology with minimal jitter. However, after initial distribution level implementation it was concluded that for the present scenario, CML distribution doesn't provide a good power vs swing trade-off.
    - Required multiple stages to distribute downstream load and ended up burning lot of power.
    - Each Tx required individual cml2cmos conversion which gives extra power hit.

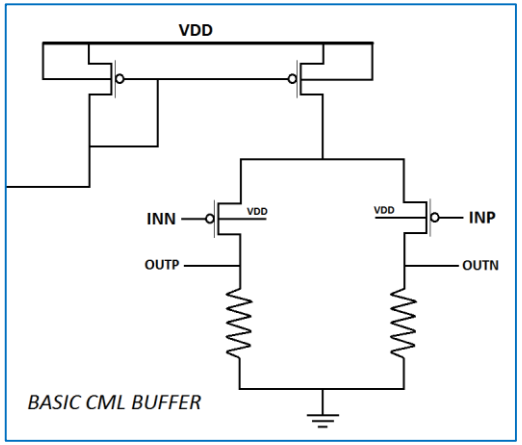
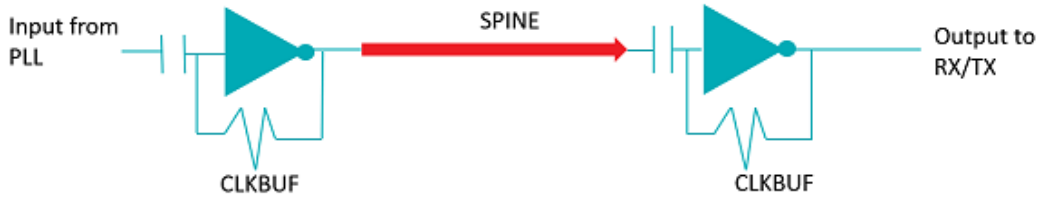


FIG 2

PROPOSED SOLUTION

PROPOSED ARCHITECTURE

- VML (Voltage Mode Logic) distribution (Fig. 3) variant was also explored due to excessive power consumption of CML design.
  - Power requirements were significantly less (~50%) than CML with lower device count. The prime reason being VML burns power during toggling, whereas CML requires a constant current burn independent of signal toggling.
  - Designer gets an option to perform Individual phase power gating to disable one phase distribution. Rx/Tx can create local differential signal and save the long spine distribution power for one phase.
  - More Jitter prone as CMRR (Common Mode Rejection Ratio) is less due to its dependency on voltage variation compared to CML variant.

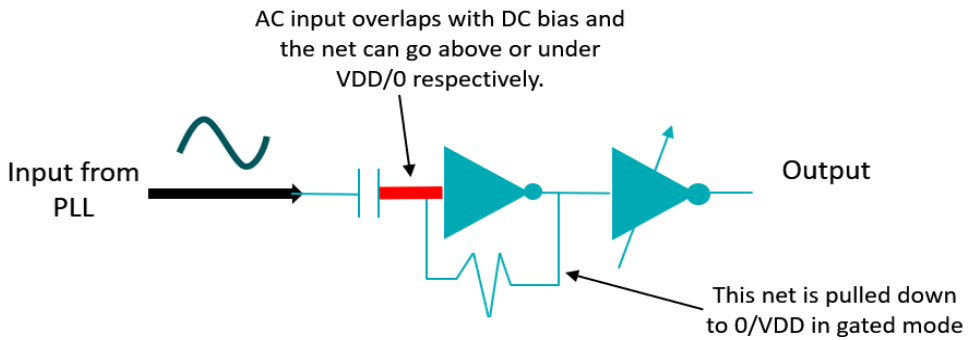


FUNCTIONAL OVERVIEW

FIG 3

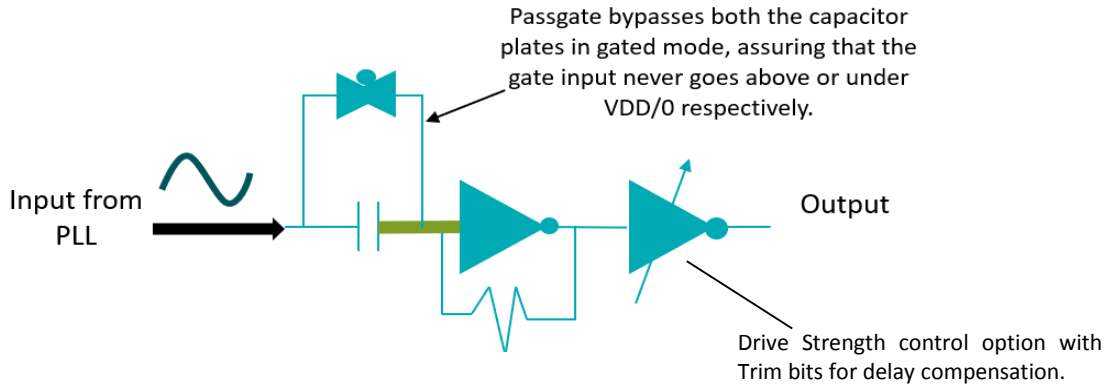
CUSTOM MODIFICATIONS

- AC Coupled inverter was followed by traditional CMOS inverter logics connected in parallel for drive strength control.
- Reliability concerns arrived during gating mode when clock buffers are gated but PLL is not due to power down sequencing.
- A bypass transmission gate was added parallel to the AC cap to kill the VDD/VSS reference coupling in gating state. This ensures that the other side net doesn't exceed VDD/VSS voltage.



BEFORE FIX

(net voltage exceeding above VDD and under VSS)



AFTER FIX

(net voltage remain within VDD/VSS)

FIG 4

RESULTS

FINAL DISTRIBUTION PLAN

- Based on the analysis from different distribution plans, a final variant was created which was taken as a trade off between number of buffer instantiations and horizontal route blockage.
- Transmission Line modeling was performed to take into account of signal reflections (if any).

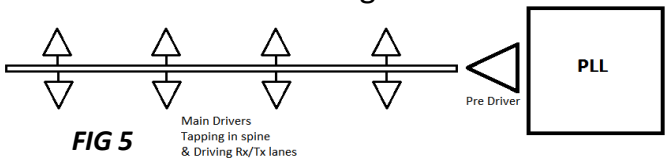


FIG 5

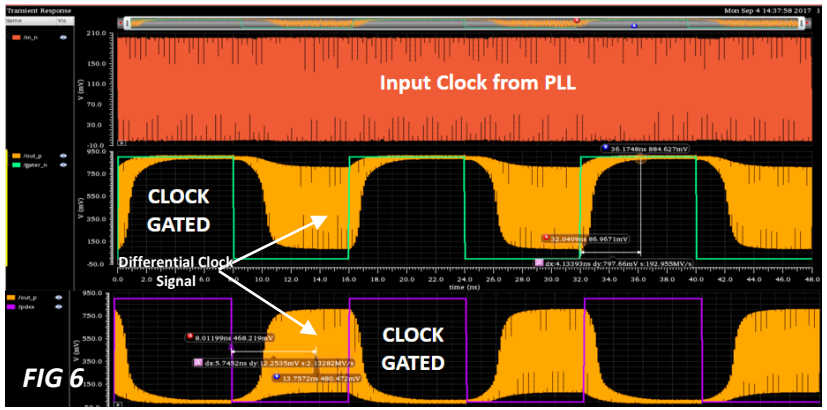


FIG 6

CLOCK GATING/SWING/SKEW ANALYSIS ACROSS CORNERS

- Differential clock gating was another requirement to make sure that functionally the clock remains clean even when it is gated. (Fig. 6)
- Cross PVT corner runs with actual LDO noise profile in the supply, were executed to meet stringent minimum swing *(~250mV Single Ended pk2pk)* and signal jitter requirements. Trim settings for swing controllability in silicon were documented. (Fig. 7)
- Clock Skew were noted across PVT and route plan adjustments executed to keep them minimum. (Fig. 8)
- Monte Carlo runs confirmed the yield confidence level.

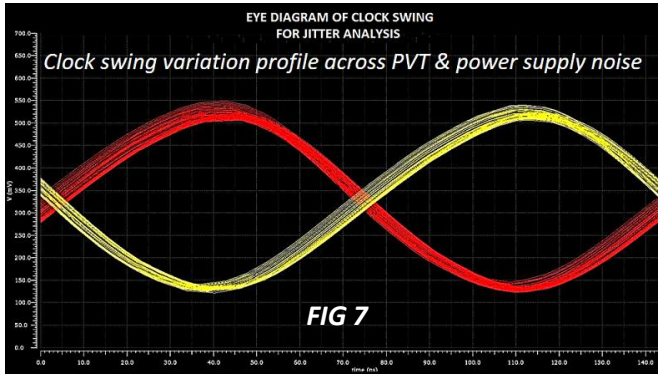


FIG 7

FIG 8

LAYOUT OPTIMIZATIONS

- For such power/noise critical design, layout played a crucial role. Utmost care was taken for clock routes with proper shielding and track planning.

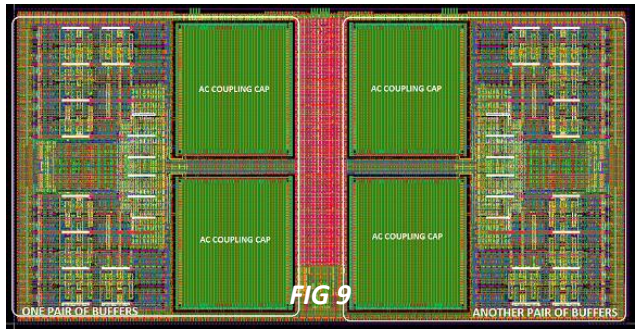


FIG 9

MONTE CARLO RUNS (SWING/DUTY-CYCLE)

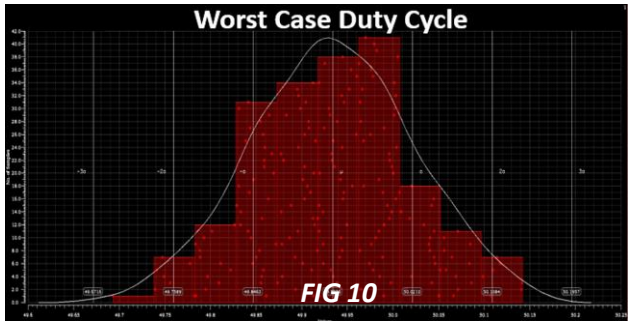


FIG 10

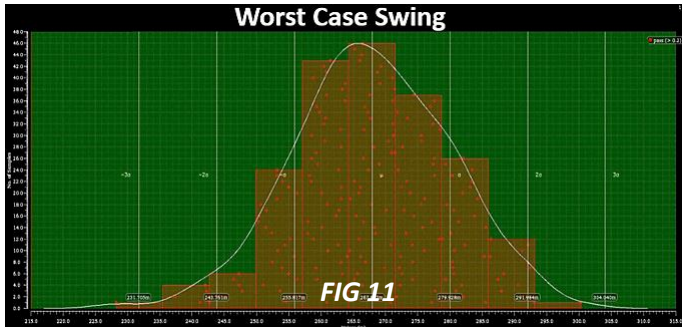
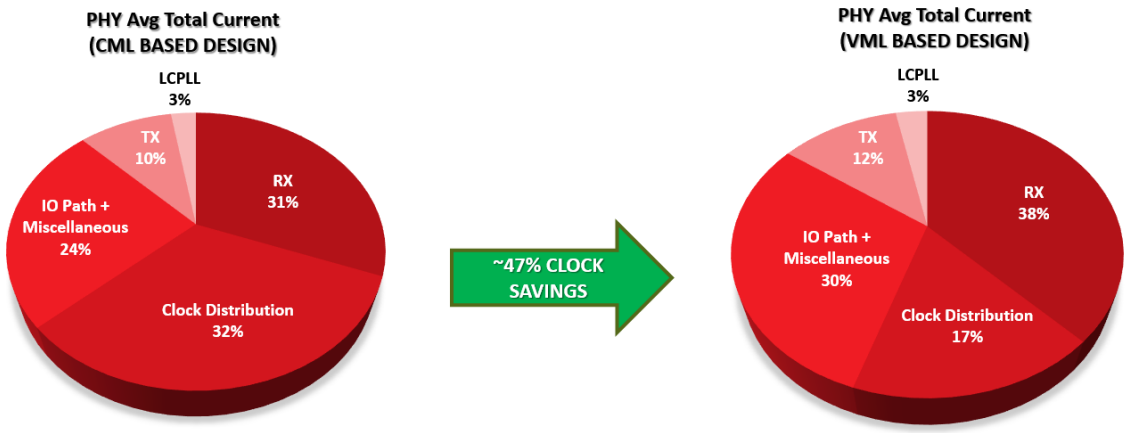


FIG 11

CONCLUSION

CLOCK POWER SAVINGS WITH JITTER TRADE-OFF

- As mentioned in the initial slides, CML type clock distribution was the favorite candidate initially due to it's low swing and high supply noise rejection ratio.
  - However, as the design progressed, it was found that the CML architecture implementation at such high frequency costed excessive power burn, above the allotted budget.
- Modified VML circuit provided much higher power savings **(~47%)**. But, at the expense of jitter (As high as 2x times compared to CML).
  - However, the design has tunability on the signal amplitude to help prioritize between power and jitter based on silicon performance as well as target product specs.



BENEFITS

APPLICABLE ACROSS INDUSTRY

- Balanced power & performance targets are crucial for any product. Proposed circuit architecture for high frequency clocking (~8GHz) was able to help reach product power goal within performance specs.

POWER SAVINGS

- Significantly lower clock power consumptions **(47% savings)** was achieved for a high frequency clock distribution compared to traditional low-swing CML type distribution.

SERDES/DDR impact

- By challenging legacy jitter targets in PHY, this power improvement solution is a clear winner and sets a good example of how we can target a better trade-off in power & performance than historically achieved.

25x20 ENERGY EFFICIENCY INITIATIVE

- Acts as another stepping stone towards the bold goal set by AMD to deliver at least 25x more energy efficiency by the year 2020 with SoCs.

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